App: Serial No. 09/833,247 Docket No. AMDA.486PA (TT4000) Amendment after Allowance

Page 2 of 3

In the Specification

At pages 5-6, lines 18-23 and 1-5 respectively, please amend the paragraph as follows:

In one particular example embodiment of the present invention, a dual FIB and electron beam (e-beam) tomography tomography device is used to effect both the substrate removal and the capturing of images from a selected portion of a semiconductor die. The dual FIB/e-beam device is used to direct a FIB at a selected portion of substrate in the die. An etch gas selected to enhance the removal of substrate from the die is introduced to the die with the FIB. The dual FIB/e-beam device is used to direct an electron beam at the die, and the interaction of the electrons with the die is used to create an image of the die. For example, the e-beam is suitable for creating an image via scanning electron microscopy (SEM). The images taken are used to form a three-dimensional image of the die, and the three-dimensional images are viewed from one or more selected angles to determine the spatial manifestations of the defect.

At page 6, lines 6-14, please amend the paragraph as follows:

In one particular implementation, the present invention is used in connection with defect analysis and identification methods used to identify a defective resistive interconnect. Resistive interconnects are often developed as a result of a void in conductive material used for the interconnect. For an example manner in which to identify a resistive interconnect, reference may be made to U.S. Patent Application Serial No. 09/586,518 (AMDA.455PA/TT3843), entitled "Resistivity Analysis" and filed on June 2, June 6, 2000, which is incorporated herein by reference. In this example methodology, suspect circuitry in a semiconductor die is identified by using a state-changing operation of the circuitry to cause a failure due to the suspect circuitry. Using this state-changing operation, one of the circuit paths that electrically changes in response to heat is identified; a particular circuit portion therein is identified as being defective because it is resistive. Once a resistive interconnect is identified, the interconnect is accessed and imaged in a manner not inconsistent with the various example embodiments described herein.